

## CLAIMS

### WHAT IS CLAIMED:

1. A method for determining one or more error conditions in a system,  
comprising:  
5           operating a device in the system in a first state;  
              modifying at least one operational characteristic of the device to operate in a  
              second state; and  
              determining if an error condition occurs in the system in response to  
              modifying the operational characteristic of the device.  
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2. The method of claim 1, wherein modifying the operational characteristic of the  
device comprises reducing the number of transactions that may be processed by the device  
during a preselected interval when in the second state.
- 15       3. The method of claim 1, wherein modifying the operational characteristic of the  
device comprises adjusting a number of transaction identifiers that are available to the device  
during the second state.
- 20       4. The method of claim 1, wherein modifying the operational characteristic of the  
device comprises adjusting a number of target identifiers that are available to the device  
during the second state.
5. The method of claim 1, wherein modifying the operational characteristic of the  
device comprises introducing non-uniform delays into the system during the second state.

6. The method of claim 1, wherein modifying the operational characteristic of the device comprises adjusting at least one of a number of secondary transfer buffer transactions, victim rewrite buffer transactions, and slave broadcast invalidates that are available during a preselected interval.

7. A system, comprising:

a control unit adapted to provide a control signal;

a first device adapted to generate one or more requests; and

a second device adapted to process one or more requests from the first device using a first configuration and adapted to process one or more requests using a second configuration in response to receiving the control signal.

8. The system of claim 7, wherein the second device comprises a FIFO queue, and wherein the first configuration of the second device comprises a pointer of the FIFO queue configured to a first level and the second configuration comprises the pointer of the FIFO queue pointer configured to a second level.

9. The system of claim 7, wherein the second configuration of the second device processes the one or more requests at a slower rate than in the first configuration.

10. The system of claim 7, wherein the second device comprises an arbiter that arbitrates at a preselected rate in the first configuration and at a rate slower than the preselected rate in the second configuration.

11. The system of claim 7, wherein the second device comprises an anti-starvation logic to gain control of a bus, and wherein the second configuration comprises the second device employing the anti-starvation to access the bus during an interval the bus is not being asserted by the first device.

12. The system of claim 7, wherein the first configuration of the second device comprises a preselected number of available transaction identifiers and wherein the second configuration comprises less than the preselected number of available transaction identifiers.

13. The system of claim 7, wherein the first configuration of the second device comprises a preselected number of available target identifiers and wherein the second configuration comprises less than the preselected number of available target identifiers.

14. An article comprising one or more machine-readable storage media containing instructions that when executed enable a processor to:

operate a device in the system in a first state;

modify at least one operational characteristic of the device to operate in a

second state; and

determine if an error condition occurs in the system in response to modifying the operational characteristic of the device.

15. The article of claim 14, wherein the instructions when executed enable the processor to reduce the number of transactions that may be processed by the device for a preselected interval during the second state.

5 16. The article of claim 14, wherein the instructions when executed enable the processor to adjust a number of transaction identifiers that are available to the device during the second state.

10 17. The article of claim 14, wherein the instructions when executed enable the processor to adjust a number of target identifiers that are available to the device during the second state.

15 18. The article of claim 14, wherein the instructions when executed enable the processor to introduce non-uniform delays into the system during the second state.

20 19. An apparatus, comprising:  
an interface; and  
a verification module adapted to receive a control signal from the interface and to adjust an operating characteristic of the apparatus to exercise a system in a manner that is capable of revealing one or more error conditions in the system in response to receiving the control signal.

20. The apparatus of claim 19, further comprising a queue, wherein the verification module adjusts a number of entries that may be stored in the queue.

21. The apparatus of claim 19, wherein the verification module accesses a bus during an interval the bus is not in use.

5 22. The apparatus of claim 19, wherein the verification module reduces the number of transactions that may be processed by the apparatus for a preselected interval.

10 23. The apparatus of claim 19, wherein the verification module increases the number of transactions that may be processed by the apparatus for a preselected interval.

15 24. The apparatus of claim 19, wherein the verification module adjusts the number of responses that may be transmitted to other devices at a preselected time.